TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. 890A.0001.U1(US)

In Re Application Of: **Michael Buchmann**

Application No.	Filing Date	Examiner	Customer No.	Group Art Unit	Confirmation No.
10/691,252	10/22/2003	Bao Q. Vu	29683	2838	5455

Invention: **Voltage Multiplier With Charge Recovery**

COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on

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Dated: 12/27/05

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IN THE U.S. PATENT AND TRADEMARK OFFICE

Appl. No.:	10/691,252
Applicant:	Michael Buchmann
Filed:	October 22, 2003
TC/AU:	2838
Examiner:	Bao Q. Vu
Docket No.:	890A.0001.U1(US)
Customer No.	29683

Title: Voltage Multiplier with Charge Recovery

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APPELLANT'S APPEAL BRIEF

Sir:

Commensurate with the Notice of Appeal filed on November 1, 2005, Applicant/Appellant hereby submits this Appeal Brief to the Board of Patent Appeals and Interferences (hereinafter, the Board) under 37 C.F.R. §41.31, and a draft for the $500 appeal brief fee set forth in 37 C.F.R. §41.20(b)(1). This Appeal Brief is filed within two months from the filing date of the above-cited Notice of Appeal and the undersigned representative believes that no late fee is due. However, should the undersigned attorney be mistaken, please consider this a petition for an extension of time under 37 C.F.R. §1.136(a) or (b) that may be required to avoid dismissal of this appeal, and debit Deposit Account No. 50-1924 as appropriate.

(1) REAL PARTY IN INTEREST

The real party in interest (RPI) is Nokia Corporation of Espoo, Finland, as indicated in an assignment of the U.S. application recorded on October 22, 2003 at reel 014638 and frame 0238.

(2) RELATED APPEALS AND INTERFERENCES

There are no other pending appeals or interferences of which the undersigned representative and assignee/RPI is aware that will directly affect, be directly affected by or have a bearing on the Board's decision in this appeal.

(3) STATUS OF CLAIMS

Claims 1-8 are pending in this appeal and stand finally rejected. Claims 1-8 are reproduced in an Appendix accompanying this Brief as those claims stood finally rejected by a final Office Action dated August 1, 2005.

(4) STATUS OF AMENDMENTS

A Response Under 37 C.F.R. §41.33 and §1.116 to the claims was proposed subsequent to the Final Rejection dated August 1, 2005. The Response Under 37 C.F.R. §41.33 and §1.116 was filed on December 15, 2005. The Response proposes to amend dependent claims 5 and 6 to depend from dependent claim 4 to correct possible confusion with respect to the term "the control pulse" in claims 5 and 6. Nonetheless, the outcome of the Response Under 37 C.F.R. §41.33 and §1.116 is immaterial to the present Appeal Brief, as claims 1 and 4-7 stand and fall together in the arguments given below. Note that the claims in the Appendix also include a second version of claims 5 and 6 as amended by the Response Under 37 C.F.R. §41.33 and §1.116.

(5) SUMMARY OF CLAIMED SUBJECT MATTER

Reference may be had to FIGS. 1, 10a, 10b, and 11 for this Summary. Independent claim 1 is directed to a capacitive voltage multiplier (FIG. 1, FIG. 11) for generating voltage pulses that are higher than the supply voltage (e.g., the voltage on input 31; see page 7, lines 20-23). The multiplier (FIG. 1, FIG. 11) includes a switching capacitor circuit (21) coupled between input (31) and output (32) terminals of the multiplier. The switching capacitor circuit (21) is provided with capacitors (e.g., capacitors 11, 12, 13 of FIG. 11) and is further provided with switches (e.g., switches 1-8 of FIG. 11) for charging the capacitors (e.g., capacitors 11, 12, 13 in FIG. 11) in parallel and discharging them in series in order to deliver a high voltage pulse. See also FIGS. 10a and 10b regarding operating switches S1-S12 in order to charge capacitors C1 through C4 in parallel and discharge the capacitors C1 through C4 in series. The multiplier (FIG. 1, FIG. 11) further includes a diode chain circuit (22) coupled between the input (31) and output (32) terminals of the multiplier (FIG. 1, FIG. 11), said diode chain circuit (22) includes a diode-chain (e.g., diodes 41, 42, 43 and 102 of FIG. 11). The diode chain circuit (22) includes pumping capacitors (e.g., capacitors 51, 52, and 53 of FIG. 11) for delivering high voltage current. See also the description from page 6, line 6 to page 8, line 3.

(6) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The only grounds for rejection presented for review by the Board is whether claims 1-8 are anticipated under 35 U.S.C. §102(b) by Kazerounian et al., U.S. Patent No. 5,006,974 (hereinafter, Kazerounian). For this issue, claims 1 and 4-6 stand or fall together, claim 2 stands or falls alone, claim 3 stands or falls alone, claim 7 stands or falls alone, and claim 8 stands or falls alone.

(7) ARGUMENT

Claims 1-8 stand rejected as being anticipated under 35 U.S.C. §102(b) by Kazerounian. Claims 1 and 4-7 stand or fall together, claim 2 stands or falls alone, claim 3 stands or falls alone, and claim 8 stands or falls alone. Claim 1 is the sole independent claim.

CLAIMS 1 AND 4-7

Independent claim 1 is directed to a capacitive voltage multiplier, such as is shown in FIGS. 1 and 11. The multiplier includes a switching capacitor circuit (21) coupled between input (31) and output (32) terminals of the multiplier. The switching capacitor circuit (21) is provided with capacitors (e.g., capacitors 11, 12, 13 of FIG. 11) and is further provided with switches (e.g., switches 1-8 of FIG. 11) for charging the capacitors (e.g., capacitors 11, 12, 13 in FIG. 11) in parallel and discharging them in series in order to deliver a high voltage pulse.

The multiplier also includes a diode chain circuit (22) coupled between the input (31) and output (32) terminals. The diode chain circuit (22) includes a diode-chain (e.g., diodes 41, 42, 43, and 102) and pumping capacitors (e.g., capacitors 11, 12, and 13) for delivering high voltage current.

In the outstanding final Office Action, the Examiner appears to assert that the charge pump circuitry 128 and capacitors 124 of Kazerounain are equivalent to the claimed "switching capacitor circuit". Applicant respectfully disagrees. Applicant reads Kazerounian as disclosing a voltage multiplier that generates an erase voltage for an Electrically Erasable Read Only Memory (EEPROM). Abstract of Kazerounian. In Kazerounain, the element 128 (called a "switching network") and the capacitors 120, 122,

and 124 solely produce a stable reference voltage, V_{ref} on lead 118. See the discussion from col. 8, line 52 to col. 9, line 38 of Kazerounain. In particular, see col. 8, lines 65-68 of Kazerounian, where it states: "The network including capacitors 120-1 to 120-20, 122-1 to 122-10, 124-1 to 124-10 and switching network 128 controls voltage V_{REF} to a desired value." Additionally, the nonvolatile register 106 controls V_{REF} (col. 8, lines 63-65 of Kazerounian) and V_{REF} is selected (using register 106) to be a particular value using a certain process. See Kazerounian at col. 8, line 68 to col. 9, line 48 of Kazerounian. Kazerounian concludes a discussion of this process by stating that "[t]his process continues until a voltage is selected which is sufficient for erasing the EEPROM. Thereafter, the contents of nonvolatile register 106 are no longer changed, and the EEPROM is erased with the selected voltage [V_{out}]." Col. 9, lines 32-35 of Kazerounian. These elements (128, 120, 122, and 124) in Kazerounian therefore do not deliver a high voltage ***pulse***, as claimed in independent claim 1 herein.

Further, the capacitors 124 in Kazerounian are not charged in parallel and discharged in series, as recited in independent claim 1. Instead, capacitors 124 in Kazerounian are selected initially as being coupled to ground through switches 126 and then one at a time they are coupled to Vpp until an appropriate erasing voltage is produced at output 104. The output voltage 104 is adjusted in Kazerounian because the comparator 116 produces a binary output signal (a "one") on output lead 119, which causes ring oscillator circuit 124 (incorrectly marked in the drawings of Kazerounian as "123") to ring and produce the signals ϕ and $\overline{\phi}$. When $V_{out}/4$ is less than V_{ref}, the comparator produces a "zero" on output lead 119, thereby stopping the ring oscillator circuit 124. See Kazerounain at col. 8, lines 9-38.

Contrast this operation of Kazerounian with FIG. 10a of the present application, where capacitors C1 through C4 are shown being charged in parallel, and FIG. 10b of the present application, where capacitors C1 through C4 are shown being discharged in series (e.g., current would flow through C1, through C2, through C3, and then through C4). Switches 126 of Kazerounian do not appear to be able to be configured to discharge capacitors 124 in series. See FIG. 2 of Kazerounian.

Thus, it is clear that the charge pump circuitry 128 and capacitors 124 in Kazerounian do not disclose or operate as a "switching capacitor circuit (21) provided with capacitors and switches for charging the capacitors in parallel and discharging them in series in order to deliver a high voltage pulse" as recited in independent claim 1. Nonetheless, other capacitors, such as capacitors 120 and 122, exist in Kazerounian. As for capacitors 120 and 122, Kazerounian states the following:

> Also as mentioned above, lead 118 provides voltage V_{REF} to comparator 116. In one embodiment, lead 118 is coupled to voltage V_{PP} (as mentioned above, typically 12 volts) via parallel-coupled capacitors 120-1 to 120-20 and to ground via parallel-coupled capacitors 122-1 to 122-10. Lead 118 is also coupled to a plate of each of capacitors 124-1 to 124-10. The second plate of capacitors 124-1 to 124-10 is connected to either ground or voltage V_{PP} via switches 126-1 to 126-10, which are part of a switching network 128. (Capacitors 120-1 to 120-20, 122-1 to 122-10 and 124-1 to 124-10 have the same capacitance C.) The state of switches 126-1 to 126-10 is controlled by the contents of register 106, described in greater detail below. The network including capacitors 120-1 to 120-20, 122-1 to 122-10, 124-1 to 124-10 and switching network 128 controls voltage V_{REF} to a desired value.

Col. 8, lines 52-28 of Kazerounian. This recited text from Kazerounian does not disclose that capacitors 120 and 122 operate as a "switching capacitor circuit (21) provided with capacitors and switches for charging the capacitors in parallel and discharging them in series in order to deliver a high voltage pulse" as recited in independent claim 1.

It should also be noted that element 103 has capacitors, and element 103 of FIG. 2 of Kazerounian is a voltage multiplier as also shown in FIG. 1 of Kazerounian. (Note that certain capacitors in voltage multiplier 103 are also marked with a "103".) Although there are a number of capacitors 103 in the voltage multiplier 103 in Kazerounian, the capacitors 103 do not appear to be charged in parallel and discharged in series and instead are operated using ϕ and $\overline{\phi}$. See, e.g., Kazerounain at col. 8, lines 9-38.

Consequently, Kazerounian does not disclose at least the recited subject matter in independent claim 1 of "wherein the multiplier comprises a switching capacitor circuit (21) coupled between input (31) and output (32) terminals of the multiplier, said switching capacitor circuit (21) provided with capacitors and *switches for charging the capacitors in parallel and discharging them in series in order to deliver a high voltage pulse*" (emphasis added). Therefore, Applicant respectfully submits that independent claim 1 is patentable over Kazerounian. Because independent claim 1 is patentable, dependent claims 4-7 are also patentable for at least the reasons given above with respect to independent claim 1.

CLAIM 2

Claim 2 recites the following: "Capacitive voltage multiplier according to claim 1, characterised in that when high voltage pulse is desired in the switching capacitor circuit (21) the series coupling switches (odd) are activated by a control pulse and all other switches (even) are opened and that in stand-by mode (no pulse) the series coupling switches (odd) are open and all other switches (even) are closed in order to charge the pump capacitors from the supply voltage, and that charge sharing will occur with the charge including the load capacitance (103)." In FIGS. 10a and 10b, the "series coupling

switches" would be S2, S4, S8, S6, and S10, while the "other switches" are switches S1, S3, and S5.

Kazerounian does not disclose that when a high voltage pulse is desired in the switching capacitor circuit, the series coupling switches (odd) are activated by a control pulse and all other switches (even) are opened. By contraindication, it appears in Kazerounian that the single set of switches 126 exist to modify V_{REF}: "The network including capacitors 120-1 to 120-20, 122-1 to 122-10, 124-1 to 124-10 and switching network 128 controls voltage V_{REF} to a desired value." Col. 8, lines 65-68 of Kazerounian. In Kazerounian, there two sets of switches, the "series coupling switches" and "other switches" as in claim 2, do not exist; instead, Kazerounian has a single set of switches 126.

For at least these reasons, dependent claim 2 is patentable over Kazerounian.

CLAIM 3

Dependent claim 3 recites "Capacitive voltage multiplier according to claim 1, characterised in that the switches of the switching capacitor circuit (21) are MEMS switches." The Examiner makes no explicit rejection in the outstanding final Office Action as to where in Kazerounian this subject matter may be found. Thus, it is unclear as to what is the specific rejection to claim 3. Nonetheless, Kazerounian does not disclose use of micromechanical (MEMS) switches. Applicant states the following at page 1, line 32 to page 2, line 2 of Applicant's specification:

> An example of an improved variant of the Marx multiplier called the Mosmarx multiplier was given by P.E.K.Donaldsen: "The Mosmarx voltage multiplier", Electronics & Wireless World, August 1988, pages 748-750. Here metal oxide semiconductors (MOS) switches were

> used instead of spark gaps. When continuous output is needed high voltage charge is stored in a separate reservoir capacitor, isolated by a serial diode from the output stage, and the switches are operated continuously. The continuous operation prevents the use of micromechanical (MEMS) switches which have a limited lifetime and/or operating frequency.

Applicant further states the following:

> Further, the first voltage multiplier 21 may be of any switching capacitor circuit type suitable for use in voltage multipliers, and the second multiplier 22 can for example be of Crockton-Walton type, but also be of any other type of diode-chain multiplier circuit. Further, instead of semiconductor switches also relays or MEMS (micro electro-mechanical system) switches may be advantageously be used to operate at least the multiplier 21.
>
> In the foregoing a novel method of interconnecting only slightly modified standard voltage multipliers has been presented giving numerous advantages, like decreasing the size of the needed capacitors, and enabling cost effective solutions like the use of MEMS switches, ***hitherto not used in voltage multipliers***, to be employed in future handheld terminals.

Page 7, line 30 to page 8, line 3 (emphasis added) of Applicant's specification. Thus, an exemplary advantage the disclosed invention is that an embodiment allows the use of MEMS switches.

Because Kazerounian does not disclose that MEMS switches may be used for switches 126 of Kazerounian and because the Applicant has shown an embodiment able to use MEMS switches when such switches were not used before in such a configuration, Applicant respectfully submits that dependent claim 3 is patentable over Kazerounian.

CLAIM 8

Dependent claim 8 recites "Capacitive voltage multiplier according to claim 1, characterised in that a supply voltage input diode (101) is used for the switching capacitor circuit (21) allowing the initial voltage of the pump capacitors to be higher than

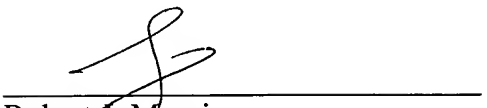
the incoming supply voltage." Assuming for sake of argument that the elements 124, 126 (and perhaps 120 and 122) are equivalent to a "switching capacitor circuit" in dependent claim 8, one can easily see in FIGS. 2 and 2a of Kazerounian that there is no diode in the part of the circuit having elements 124, 126 (and containing perhaps 120 and 122). For at least these reasons, dependent claim 8 is patentable over Kazerounian.

CONCLUSION

For at least the above reasons, the Applicant/Appellant contends that claims 1-8 are patentable over Kazerounian. The Applicant/Appellant respectfully requests the Board reverse the final rejection in the Office Action of August 1, 2005, and further that the Board rule that the pending claims are patentable over the cited art.

Respectfully submitted:

HARRINGTON & SMITH, LLP



12/27/05

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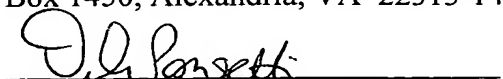

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(8) CLAIMS APPENDIX

1. Capacitive voltage multiplier for generating voltage pulses, preferably up to 100 V, that are higher than the supply voltage for displays, non-volatile memories and corresponding units especially in small electronic devices, such as handheld telecommunication terminals or corresponding devices,

wherein the multiplier comprises a switching capacitor circuit (21) coupled between input (31) and output (32) terminals of the multiplier, said switching capacitor circuit (21) provided with capacitors and switches for charging the capacitors in parallel and discharging them in series in order to deliver a high voltage pulse,

characterised in that the multiplier further comprises a diode chain circuit (22) coupled between said input (31) and output (32) terminals of the multiplier, said diode chain circuit (22) comprising a diode-chain and pumping capacitors for delivering high voltage current.

2. Capacitive voltage multiplier according to claim 1, characterised in that when high voltage pulse is desired in the switching capacitor circuit (21) the series coupling switches (odd) are activated by a control pulse and all other switches (even) are opened and that in stand-by mode (no pulse) the series coupling switches (odd) are open and all other switches (even) are closed in order to charge the pump capacitors from the supply voltage, and that charge sharing will occur with the charge including the load capacitance (103).

3. Capacitive voltage multiplier according to claim 1, characterised in that the switches of the switching capacitor circuit (21) are MEMS switches.

4. Capacitive voltage multiplier according to claim 1, characterised in that the output of the switching capacitor circuit (21) is activated at the start of a control pulse.

NOTE: Claim 5 stood finally rejected by a final Office Action dated August 1, 2005 as follows:

5. Capacitive voltage multiplier according to claim 1, characterised in that an output of the switching capacitor circuit (21) is not coupled via a diode to the output terminal (32) of the multiplier so that current at the end of the control pulse can flow back into the pump capacitors, whereby the charge in the load capacitor is partly restored in the pumping capacitors.

NOTE: In Response Under 37 C.F.R. §41.33 and §1.116, dated December 15, 2005, claim 5 was amended as follows:

5. Capacitive voltage multiplier according to claim ~~1~~4, characterised in that an output of the switching capacitor circuit (21) is not coupled via a diode to the output terminal (32) of the multiplier so that current at the end of the control pulse can flow back into the pump capacitors, whereby the charge in the load capacitor is partly restored in the pumping capacitors.

NOTE: Claim 6 stood finally rejected by a final Office Action dated August 1, 2005 as follows:

6. Capacitive voltage multiplier according to claim 1, characterised in that the diode chain circuit (22) is continuously operated during the control pulse duration and holds the output voltage at a fixed level.

NOTE: In Response Under 37 C.F.R. §41.33 and §1.116, dated December 15, 2005, claim 6 was amended as follows:

6. Capacitive voltage multiplier according to claim ~~1~~4, characterised in that the diode chain circuit (22) is continuously operated during the control pulse duration and holds the output voltage at a fixed level.

7. Capacitive voltage multiplier according to claim 1, characterised in that the diode chain circuit (22) output is through a diode (102) and that no reservoir capacitor is used.

8. Capacitive voltage multiplier according to claim 1, characterised in that a supply voltage input diode (101) is used for the switching capacitor circuit (21) allowing the initial voltage of the pump capacitors to be higher than the incoming supply voltage.

END OF CLAIMS

(9) EVIDENCE APPENDIX

There is no evidence submitted pursuant to 37 C.F.R. §§1.130, 1.131, or 1.132 or entered by the Examiner and relied upon by Appellant.

(10) RELATED PROCEEDING APPENDIX

There are no known decisions rendered by a court or the Board in any proceeding identified pursuant to paragraph (c)(1)(ii) of 37 C.F.R. §41.37.